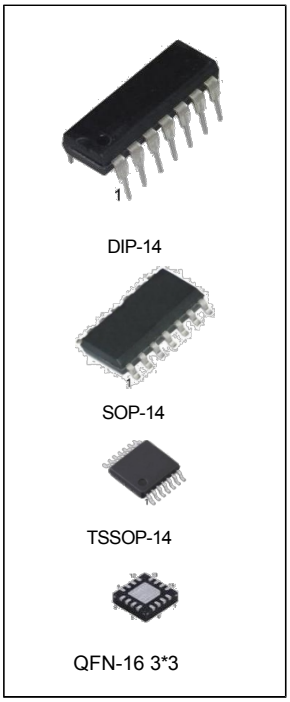
Product Description

The CD4069UB is a low-power, wide operating voltage inverter designed with advanced CMOS technology. It integrates six mutually independent inverter circuits internally with high immunity and drive capability.



Product Features

- Low input current: IIN≤1uA, @ VIN=VDD=15V,Ta=25°C
- Wide operating voltage range: 3.0V to 15.0V
- Low static power consumption: IDD≤4uA,@VDD=15V,Ta=25°C
- Package: DIP-14, SOP-14, TSSOP-14, QFN-16 3*3

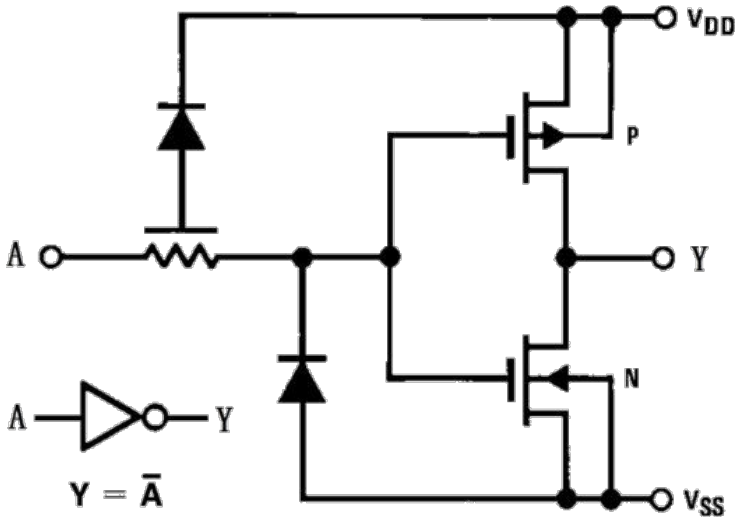
Product Use

- Digital logic driver
- Industrial Control Applications
- Wireless Doorbell
- Other application areas

Product Ordering Information

Product name	Encapsulation	Print Name	Package	Packing quantity
CD4069UBE/ CD4069UBN	DIP-14	CD4069UB	TUBE	1000 per box
CD4069UBM/TR	SOP-14	CD4069UB	REEL	2500 per REEL
CD4069UBMT/TR	TSSOP-14	CD4069UB	REEL	2500 per REEL
CD4069UBLQ/TR	QFN-16 3*3	CD4069UB	REEL	5000 per REEL

Schematic



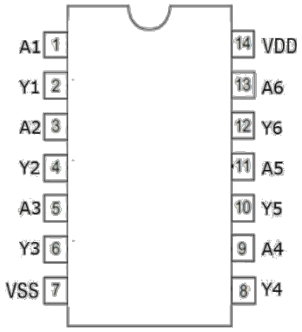
Truth table

Input	Output
A	Y
L	H
H	L

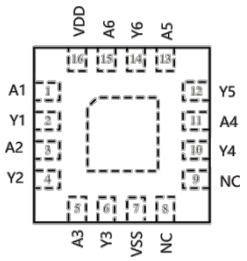
H = High Logic Level

L = Low Logic Level

Package Format and Pin Function



dip-14/sop-14/tssop-14



QFN-16 3*3

Pin Function

Pin		Symbol	Description
DIP/SOP/TSSOP	QFN-16		
1	1	A1	Data input 1
2	2	Y1	Data output 1
3	3	A2	Data input 2
4	4	Y2	Data output 2
5	5	A3	Data Input 3
6	6	Y3	Data output 3
7	7	VSS	Ground (0V)
8	10	Y4	Data output 4
9	11	A4	Data input 4
10	12	Y5	Data output 5
11	13	A5	Data Input 5
12	14	Y6	Data output 6
13	15	A6	Data input 6
14	16	VDD	Supply Voltage
-	8	NC	No internal connections
-	9	NC	No internal connections

Limit parameters

Parameter name	Symbol	Limit	Unit
Supply Voltage	VDD	-0.5-18	V
Input Voltage	VIN	-0.5+VSS-VDD+0.5V	V
power wastage	PD	500	mW
operating temperature	TA	-40~85	°C
Storage temperature	TS	-65-150	°C
Pin Soldering Temperature	TW	260,10s	°C

Note: Limit parameter refers to the limit value that cannot be exceeded under any condition. If the limit value is exceeded, it may cause physical damage such as product deterioration; at the same time, it is not guaranteed that the chip can work normally under the near limit parameter.

Recommended working conditions

Parameter name	Symbol	Minimum	Typical	Maximum	Unit
operating voltage	VDD	3		15	V
Input and output voltage	V_{IN}, Vout	0		VDD	V
operating temperature	TA	-40		85	°C

Electrical Characteristics DC Electrical Characteristics. TA=25°C

Symbo	Parameter name	Test condition		VDD (V)	Minimum	Typical	Maximum	Unit
VIH	High-level active input voltage	$\|I_O\| \leq 1uA$	Vo=0.5V	5	4.0			V
			Vo=1V	10	8.0			V
			Vo=1.5V	15	12.0			V
VIL	Effective low level input voltage	$\|I_O\| \leq 1uA$	Vo=4.5V	5			1.0	V
			Vo=9V	10			2.0	V
			Vo=13.5V	15			3.0	V
VOH	High Level Output Voltage	|IOUT|<1uA		5	4.95			V
				10	9.95			V
				15	14.95			V
VOL	Low Level Output Voltage	|IOUT|<1uA		5		0	0.05	V
				10		0	0.05	V
				15		0	0.05	V
IIN	Input Current	V_{IN} = VVDD or VSS		15		0	1.0	uA
IOH	High Level Output Current	Vo= 4.5V		5		-1.4	-0.45	mA
		Vo= 9V		10		-3.0	-1.2	mA
		Vo= 13.5V		15		-10	-3	mA
IOL	Low Level Output Current	Vo= 0.4V		5	0.45	3.3		mA
		Vo= 0.5V		10	1.0	12		mA
		Vo= 1.5V		15	3.0	24		mA
IDD	Operating Current	V_{IN} = VVDD or VSS		5			1.0	uA
				10			2.0	uA
				15			4.0	uA

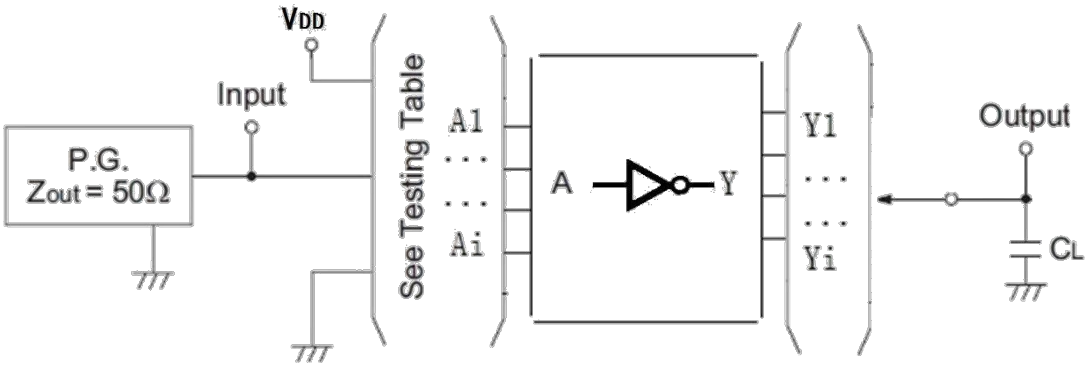
AC Electrical Characteristics.

Ta=25°C ,see test method.

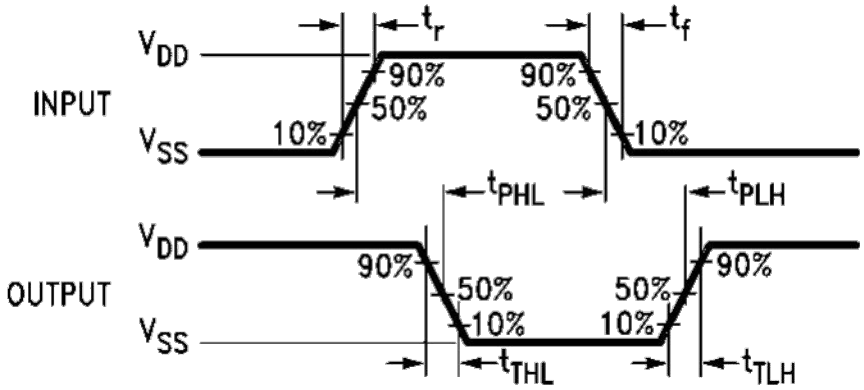
Parameter name	Symbol	Test condition	Minimum	Typical	Maximum	Unit
Transmission delay time A to Y	tPHL	VDD=5V CL=51pF		32		ns
	tPLH			42		ns
	tPHL	VDD=10V CL=51pF		23		ns
	tPLH			32		ns
	tPHL	VDD=15V CL=51pF		25		ns
	tPLH			27		ns

Test Methods

Test Wiring Diagram



Waveform Measurement Schematic



Note: 1. See Testing Table refers to the corresponding test items in the AC electrical characteristics table;

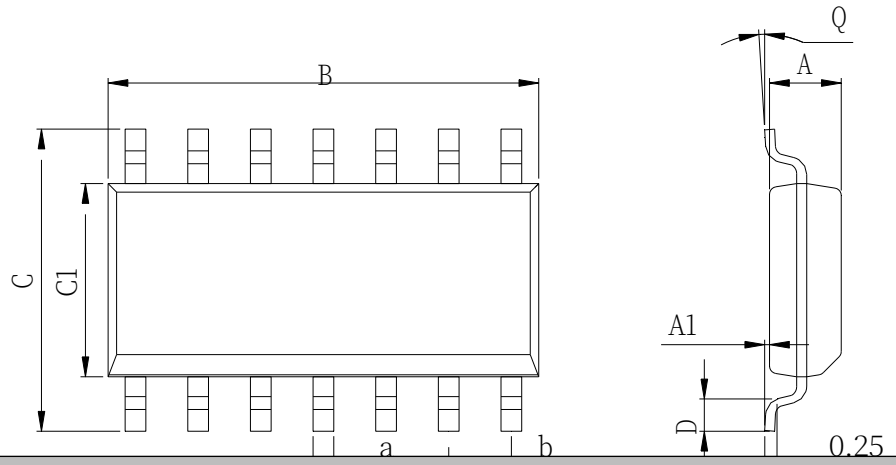
2, CL capacitance for external chip capacitor (0603) near the output pin access, capacitance ground near the chip VSS;

3, Input: Port input level, f=1MHz,D=50% square wave, tr=tf≤20ns;

4. Output: Y-end output test.

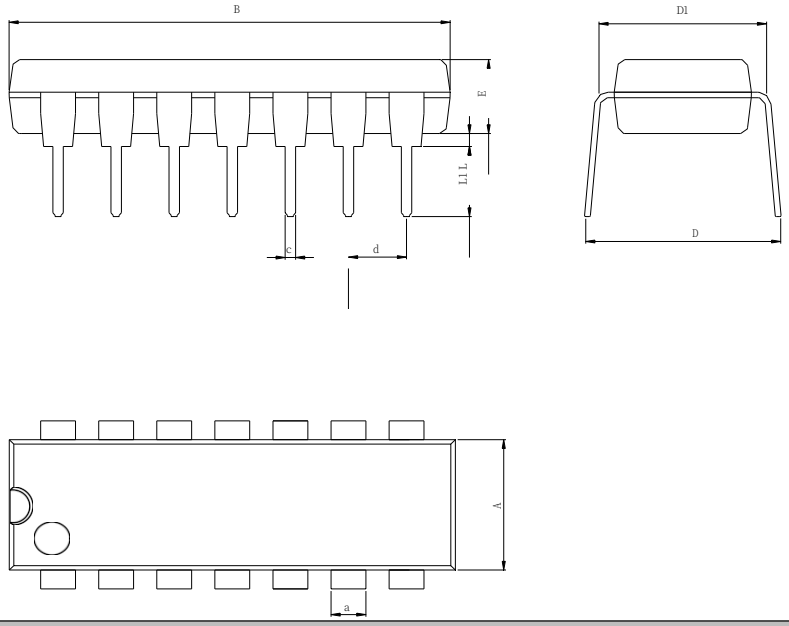
Package Outside Dimensions

SOP-14



Dimensions In Millimeters (SOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	8.55	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	8.75	6.20	4.00	0.80	8°	0.45	

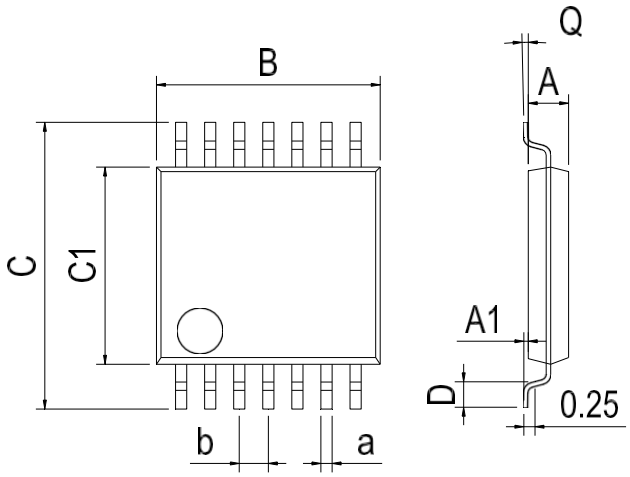
DIP-14



Dimensions In Millimeters (DIP-14) Symbol:	A									
	B	AB		D1	E	L	L1	a	c	d
Min:	6.10	18.94	8.10	7.42	3.10	0.50	3.00	1.50	0.40	2.54 BSC
Max:	6.68	19.56	10.9	7.82	3.55	0.70	3.60	1.55	0.50	

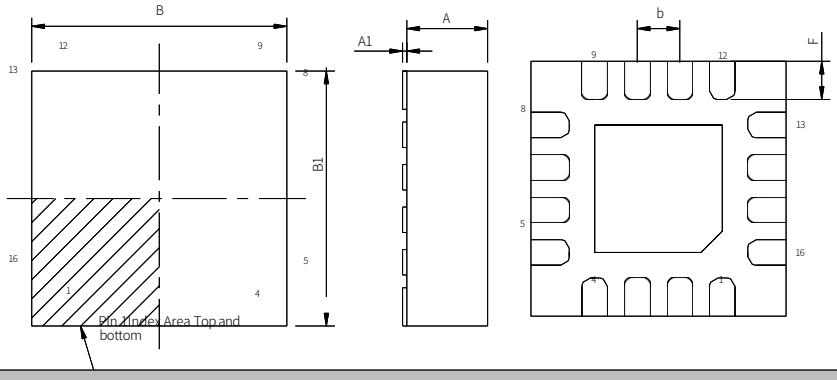
Package Outside Dimensions

TSSOP-14



Dimensions In Millimeters(TSSOP-14)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.85	0.05	4.90	6.20	4.30	0.40	0°	0.20	0.65 BSC
Max:	0.95	0.20	5.10	6.60	4.50	0.80	8°	0.25	

QFN-16 3*3



Dimensions In Millimeters (QFN-16 3*3)								
Symbol:	A	A1	B	B1	E	F	a	b
Min:	0.85	0	2.90	2.90	0.15	0.25	0.18	0.50TYP
Max:	0.95	0.05	3.10	3.10	0.25	0.45	0.30	

revision history (of a document, web page etc)

dates	Content of the modification	pagination
2019-12-8	new amendment	1-8
2023-11-14	Updated Packages, Updated DIP-14 Dimensions, Updated DIP Package New Models	1, 6
2024-11-8	QFN-16 Package Type Added, Pin Soldering Temperatures Updated	1, 4

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